Peter E. Bailey

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Education

PhD computer science, expected December 2015
Thesis: "*Power-Constrained Performance in Supercomputing"*
Electrical engineering minor
University of Arizona
Advisor: David Lowenthal

MS electrical engineering, computer science minor, June 2009
Institute of Technology, University of Minnesota
Advisor: David Lilja

BS computer engineering, cum laude, May 2008
Institute of Technology, University of Minnesota

Interests

High-performance & parallel computing, energy-efficient computing, GPUs, accelerators, runtime systems, compilers.

Refereed Conference and Workshop Publications

P E Bailey, A Marathe, D K Lowenthal, B Rountree, M Schulz, B R de Supinski, "*Finding the Limits of Power-Constrained Application Performance*," in submission, 2015.

A Marathe, **P E Bailey**, D K Lowenthal, B Rountree, M Schulz, B R de Supinski, "*A Run-Time System for Power-Constrained HPC Applications*," ISC-2015: International Supercomputing Conference, Frankfurt, Germany, 2015 (to appear).

A Randles, E W Draeger, **P E Bailey,** "Massively Parallel Simulations of Hemodynamics in the Primary Large Arteries of the Human Vasculature," ICCS-2015: International Conference on Computational Science, Reykjavik, Iceland, 2015. **Best paper award.**

P E Bailey, D K Lowenthal, V Ravi, B Rountree, M Schulz, B R de Supinski, "*Adaptive Configuration Selection for Power-Constrained Heterogeneous Systems*," ICPP-2014: 43rd International Conference on Parallel Processing, Minneapolis, MN, USA, 2014.

P E Bailey, T Patki, G M Striemer, A Akoglu, D K Lowenthal, P Bradbury, M Vaughn, L Wang, S Goff , "*Quantitative Trait Locus Analysis Using a Partitioned Linear Model on a GPU Cluster,*" Parallel and Distributed Processing Symposium Workshops & PhD Forum (IPDPSW), 2012 IEEE 26th International, pp.752-760, 21-25 May 2012

P E Bailey, J Myre, S D C Walsh, D J Lilja, M O Saar, "*Accelerating Lattice Boltzmann Fluid Flow Simulations Using Graphics Processors*," in ICPP- 2009: 38th International Conference on Parallel Processing, Vienna, Austria, 2009.

S D C Walsh, M O Saar, **P E Bailey**, D J Lilja, "*Cheaper and faster: How to have your cake and eat it too with GPU implementations of Earth Science simulations*," Fall Eos Trans. AGU, 89(53), Fall Meeting Supplement, Abstract IN23C-1102, 2008.

Refereed Journal Publications

S D C Walsh, M O Saar, **P E Bailey**, D J Lilja, "*Accelerating geoscience and engineering system simulations on graphics hardware*," Comput. Geosci. 35 (2009) 2353–2364.

Patents

P E Bailey, I Paul, M Arora, "*Hardware/Runtime Coordinated Load Balancing for Parallel Applications*," submitted 2015.

Technical Reports

2007-2009: Senior honors design project and master's project. Used graphics processing cards to parallelize and speed up a computational fluid dynamics simulation, resulting in 25x performance improvement over a CPU-based version. Coded in C, C++, CUDA.

Honors

Department research fellowship, 2015
Oscar A. Schott Undergraduate Scholarship, 2007 - 2008
ECE Senior Honors Design Program, 2007 - 2008
Dean's List, University of Minnesota Institute of Technology, 2005, 2006
Ella Thorpe Math Scholarship, 2006

Technical Societies

2007 – Present: Member IEEE
2009 – Present: Member ACM

Technical Skills

Programming languages
C, C++, R, MATLAB, Python, Java, Verilog, VHDL, Lisp, various assembly languages

Software suites/methodologies
MPI, OpenMP, Nvidia CUDA, OpenCL, Pthreads

Research Experience

2010-present: **Graduate Research Associate**, Prof. David Lowenthal, advisor, Computer Science Department, University of Arizona.

2013: **Graduate Research Intern,** Advanced Micro Devices, Austin, TX. Primary author on one chapter of AMD's "Programmability" report for Exascale Fast Forward grant from U.S.

Department of Energy. See ICPP-2014 paper and 2014 patent submission.

Fall 2012, Fall 2014: **Teaching Assistant**, graduate-level parallel computing, Computer Science Department, University of Arizona.

Summer 2011: **Graduate Research Intern,** Lawrence Livermore National Laboratory, Livermore, CA. Extended power-aware MPI runtime system to machines with multiple cores per processor.

2007-2009: **Lab Teaching Assistant**, Intro to Digital Design and Intro to Microcontrollers, University of Minnesota ECE Department.

Professional Experience

2009-2010: **Software Engineer,** CAAO, Steward Observatory, Tucson, AZ. Improved hardware control reliability and UI usability for astronomical camera & interferometer operation; designed and built data storage system. C++, Java, Tcl/Tk.

2009: **Software and Configuration Engineer**, Lockheed Martin MS2, Eagan, MN. Performed software functionality and regression testing. Coordinated builds and installations of an airborne multi-workstation, multi-platform surveillance and reconnaissance application.

2008: **Programmer**, Observational Cosmology Group, University of Minnesota Physics Department. Implemented an ATA over Ethernet data backend and a custom RPC library for HW sensor data aggregation and HW control for the EBEX experiment, a balloon-borne telescope for measuring cosmic microwave background polarization. C, Python, HTTP, ATAoE.

2007: **Software Engineer Intern**, MTS Systems Corporation, Eden Prairie, MN. Improved build time and usability of an automotive testing machine interface. Reduced build time from multiple hours to 20 minutes. Coded in Visual Basic, C, C++, VBA, Excel.

2005-2007: **On-site Tech Support**, Minnesota Population Center, Minneapolis, MN.

2003, 2004: **Firmware programmer**, Micro Control Company, Fridley, MN. Implemented an embedded real-time power control and reporting system in C and assembly for a semiconductor device burn-in oven.